

File Edit V&V Code Generation View Tool Help

100%

Syntax Analysis button

Mapping_12 Mapping_22 WPD_App ZigBee_TX Mapping_0 Mapping_1 Mapping_2
DIPLODOCUS_Methodology CP_Memory_Copy DMA_transfer Double_DMA_transfer Embb Mapping_02
F_Chip2Octet X_Chip2Octet F_CWL X_CWL F_CWP_I X_CWP_I F_CWP_Q X_CWP_Q
TML Component Task Diagram F_Symbol2ChipSeq X_Symbol2ChipSeq F_Sink X_Sink F_Source X_Source

Choosing TML components to validate

Ignored components

Used components

- Primitive component: X_S
- Primitive component: F_S
- Primitive component: X_S
- Primitive component: F_S
- Primitive component: X_S
- Primitive component: F_S
- Primitive component: X_C
- Primitive component: F_C
- Primitive component: X_C
- Primitive component: F_C
- Primitive component: X_C
- Primitive component: F_C

☒ Optimize TML specification

Cancel Start Syntax Analy...

SourceReq

Symbol2ChipSeqReq

Chip2OctetReq

Source

Chip2Octet

X_Sc

+ size : Natural;

X_Chip2Octet

+ size : Natural;

F_Source

+ size : Natural;

F_Symbol2ChipSeq

+ size : Natural;

F_Chip2Octet

+ size : Natural;

Checks that all diagrams follows the TTool's syntax