

File Edit V&V Code Generation View Tool Help

Mapping\_22 WPD\_App ZigBee\_TX Mapping\_0 Mapping\_1 Mapping\_2 Mapping\_3  
DIPLODOCUS\_Methodology CP\_Memory\_Copy DMA\_transfer Double\_DMA\_transfer Emmb Mapping\_02 Mapping\_12

DIPLODOCUS architecture and mapping Diagram

Choosing Nodes to validate

Nodes ignored

Nodes taken into account

- INTL\_DMA: name
- ADAIF\_DMA: name
- ADAIF\_MSS: name
- ADAIF\_PSS: name
- ADAIF\_Bridge: name
- DDR: name
- MainCPU: name
- MainBus: name
- MainBridge: name
- Crossbar: name
- INTL\_Bridge: name
- INTL\_MSS: name

☒ Optimize TML specification

Master clock (in MHz) 200

Cancel Start Syntax Analy...

Diagram components:

- CPURR ADAIF\_PSS
- CPURR FEP\_PSS
- CPURR ADAIF\_DMA
- MEMORY FEP\_MSS
- BUS-RR ADAIF\_Bus
- BUS-RR FEP\_Bus
- BRIDGE
- ZigBee\_TX::X\_Sink
- ZigBee\_TX::X\_CWL
- ZigBee\_TX::X\_CWP\_I
- ZigBee\_TX::X\_CWP\_Q