

TC4200 WiMAX Low Density Parity Check Decoder v1.0 Datasheet SoCLib

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TC4200 is a product of TurboConcept SAS, 40 rue Joseph Fourier, 29280 PLOUZANE, FRANCE.

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DOCUMENT REVISION HISTORY

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PRODUCT VERSIONS

Date	Version	Description
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BUG HISTORY

N°	Identified in version	Description	Fixed in version

Introduction

TurboConcept's TC4200 is a versatile high speed Low Density Parity Check code (LDPC) decoder compliant with the IEEE 802.16e specifications used for WiMAX systems. The Core is a stand-alone module, with no external memory needs. It is available for mainstream FPGA or ASIC device targets. The Core covers the entire WiMAX LDPC specifications [1], in terms of block size and code rate. Block size and code rate can be switched on a block-by-block basis.

This document gives the functional and interfacing specifications. Actual device resource usage and FEC performance are provided in the device-dependant companion documentations.

1 General description

1.1 Functional overview

The Core is compliant with the LDPC code specification given in 802.16e documentation [1] section 8.4.9.2.5 (“Low Density Parity Check code (optional)”).

The detailed specification of the encoding process can be found in this reference documentation and is not recalled here.

TC4200 performs the corresponding iterative LDPC decoding. Figure 1 displays the functional block diagram of the Core.

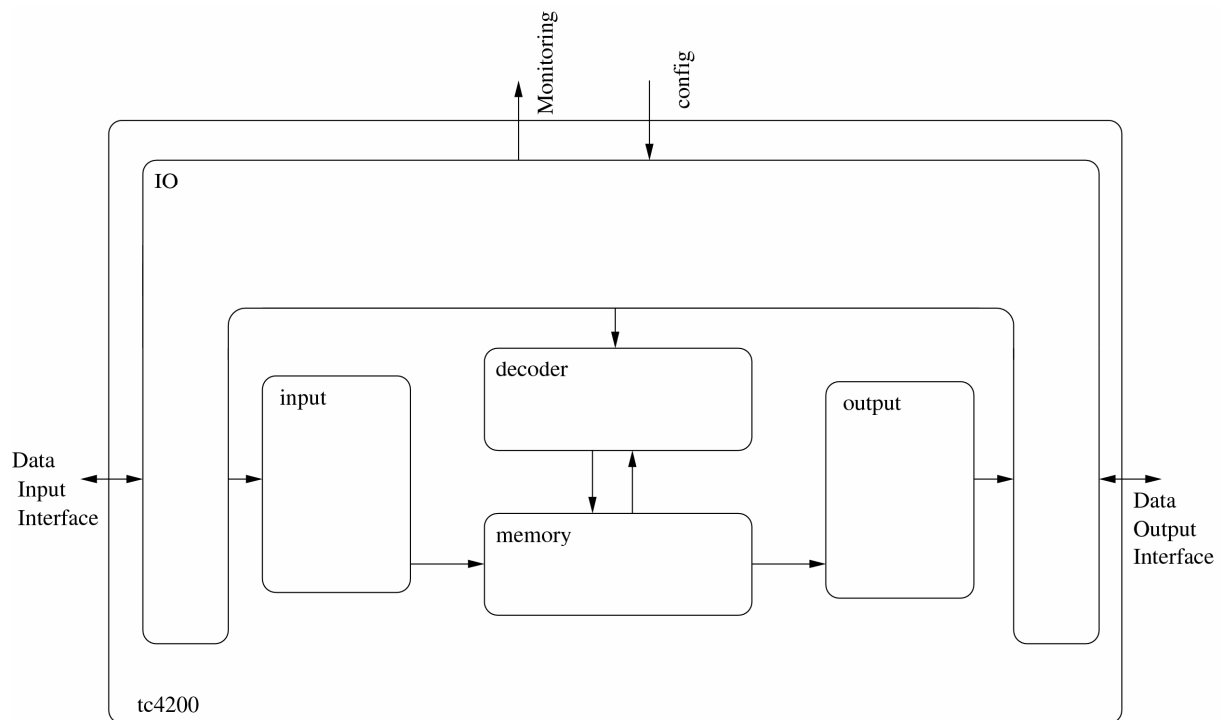


Figure 1: Functional block diagram

The Data Input Interface is used to give to the Core a set of channel observation data, in the form of quantized Log-Likelihood on coded bits (bit-LLRs).

The Data Output Interface gives the decoding result, in the form of decision bits on the payload section of the frame.

The Core is monitored and controlled through dedicated configuration pins.

The following Control facilities are available:

- WiMAX LDPC coding matrix
- Block size
- Maximum number of LDPC decoding iterations
- Use of the built-in stopping criterion

These settings can be changed dynamically for each frame. TC4200 can therefore be easily implemented in an adaptive modulation and coding system.

The following Monitoring facilities are available:

- LDPC syndrome verification and early stopping criterion
- Actual number of iteration performed by the LDPC decoder

The SoCLib model disables the maximum number of LDPC decoding iterations and the use of the built-in stopping criterion. The actual number of iteration performed is internally set to a reasonable value still offering close-to-ideal Bit Error Rate (BER) performances.

1.2 Codes supported

Table 1 gives the rates and block sizes supported. The Core covers the complete set of cases defined in [1]. Please refer to [1] for details on the “expansion factor”.

Expansion factor	Coded Block size (bits)	LDPC code rates
24	576	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
28	672	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
32	768	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
36	864	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
40	960	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
44	1056	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
48	1152	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
52	1248	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
56	1344	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
60	1440	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
64	1536	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
68	1632	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
72	1728	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
76	1824	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
80	1920	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
84	2016	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
88	2112	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
92	2208	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6
96	2304	1/2, 2/3A, 2/3B, 3/4A, 3/4B, 5/6

Table 1: Frame size and code rate supported

2 Detailed description

2.1 Block Diagram

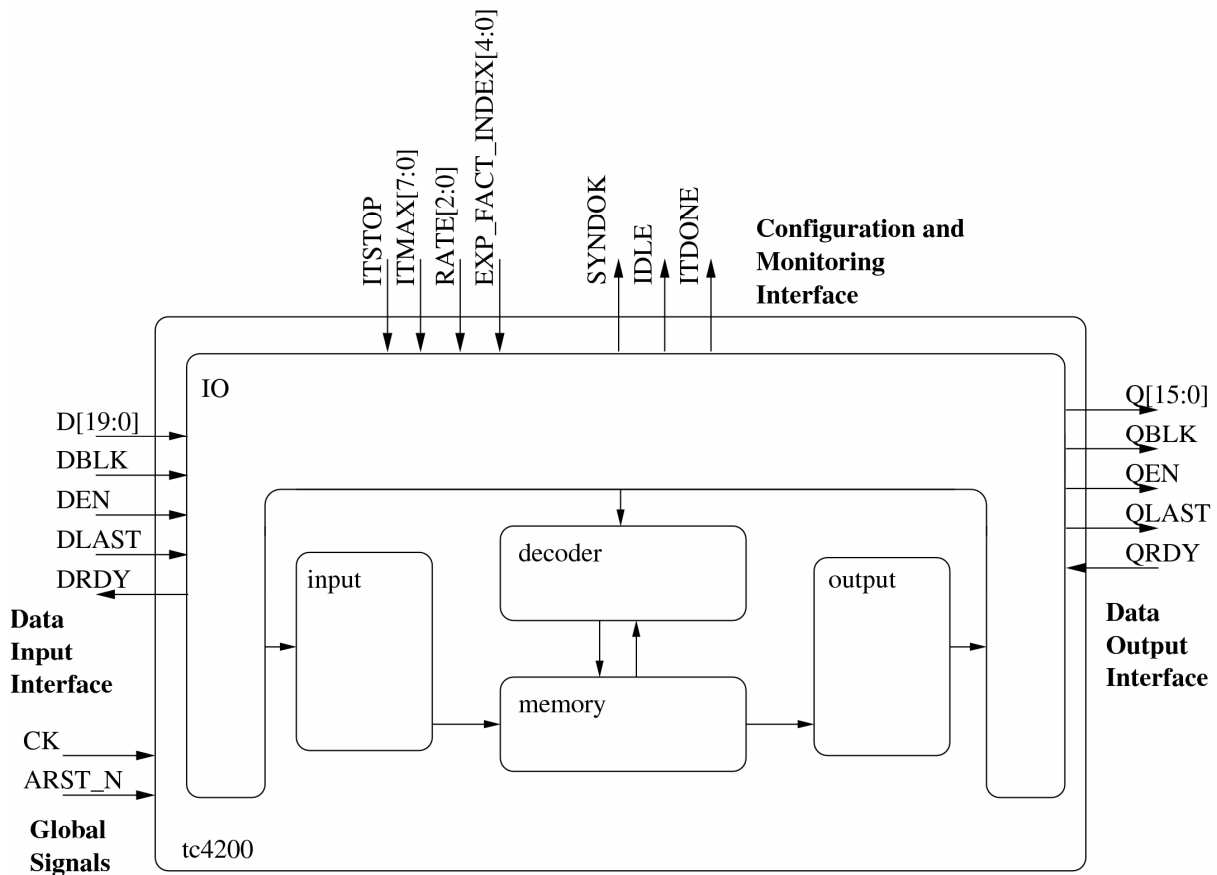


Figure 2: TC4200 block diagram

TC4200 is composed of the following modules:

- An input module handling the input interface using four parallel bit-LLR samples
- An iterative decoder module
- An output module handling the 16 bit parallel output interface
- A I/O and configuration module, handling the configuration and interfacing the TC4200 core with the external world

2.2 Block processing

A timing diagram illustrating the block processing timing is given in Figure 3. DRDY is high to indicate that the Core is ready to receive a new block. This figure illustrates the logic behavior of DRDY output pin which can be used by the user to start the next block input. While the Core is decoding a block, the input interface is ready to receive the next block to reduce the overall latency.

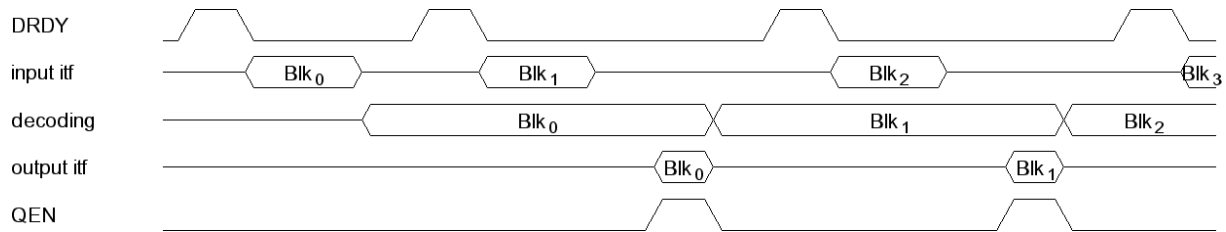


Figure 3: Block processing timings

2.3 Congestion control

Two signals are used to control the block processing and to avoid congestion:

- **QRDY** (Core input signal) asserted HIGH indicates to TC4200 that a block can be output from the Core. If QRDY is LOW, the Core will hold the data until QRDY rises.
- **DRDY** (Core output signal) asserted HIGH indicates that TC4200 is ready to receive a block.

3 Interfaces and I/Os

This section details the I/Os pins and the interfaces protocols.

3.1 Global signals

Signal name	Type	Size	Function
CK	I	1	Core clock. Please refer to the applicable application note for maximum operating frequency
ARST_N	I	1	Asynchronous Hardware reset. Active LOW.

Table 2: Global signals

3.2 Data input interface

3.2.1 Signals

All signals are considered at rising edge of the clock CK.

Signal name	Type	Size	Function
D	I	4*LLR_WIDTH	Data port in 2's complement format. Format is described in section 3.2.2
DBLK	I	1	Block start strobe. Active HIGH. Indicates a new block
DEN	I	1	Enable signal for symbols D Active HIGH
DLAST	I	1	Last data strobe: Active HIGH Activated synchronously with the current input block last data
DRDY	O	1	Ready for block input start (DBLK strobe). Active HIGH. DRDY=HIGH indicates that the Core can accept a new block input. DBLK is ignored if DRDY=LOW. DRDY is asserted LOW two clock cycles after a valid strobe on DBLK. DRDY goes high a few clock cycles after a reset operation.

Table 3: Input interface signals

3.2.2 Data size and format

Let denote by c_i the emitted code word bits, with i in $[0, n-1]$. c_0, \dots, c_{k-1} are the systematic part of the code word; c_k, \dots, c_{n-1} are the redundancy part.

Let denote by s_i the received code word bit-LLRs (Log-Likelihood Ratios), with i in $[0, n-1]$, with s_i corresponding to c_i . (s_0, \dots, s_{k-1} are the systematic part of the soft received code word; s_k, \dots, s_{n-1} are the redundancy part).

Each bit-LLR sample s_i is a 2's complement data coded using LLR_WIDTH bits.

LLR_WIDTH is set to 5.

Each s_i is in the range $[-15; +15]$.

The input data signal D carries a set of 4 s_i values, according to the correspondence below:

symbol index	D[19:15]	D[14:10]	D[9:0]	D[4:0]
0	s_0	s_1	s_2	s_3
1	s_4	s_5	s_6	s_7
..				
j	s_{4j}	s_{4j+1}	s_{4j+2}	s_{4j+3}
...				
n/4-1	s_{n-4}	s_{n-3}	s_{n-2}	s_{n-1}

Table 4: Mapping of soft bit-LLRs s_j into signal D

The size of the input bus D is $4 \times \text{LLR_WIDTH}$ ($\text{LLR_WIDTH} = 5$).

The data format for any s_i is 2's complement.

Value	Meaning
+15	Most reliable "1"
...	
+1	Least reliable "1"
0	Neutral value
-1	Least reliable "0"
...	
-15	Most reliable "0"

Table 5: Input format example with $\text{LLR_WIDTH}=5$

3.2.3 Waveform examples

Figure 4 gives a waveform example of the input interface signals. The input samples (bit-LLRs) are denoted D_0 to $D_{n/4-1}$.

The pattern on signal DEN is arbitrary chosen.

The signal DRDY falls as indicated, two cycles after the strobe on DBLK. It rises again after the previous input data block has been decoded and provided by the Core.

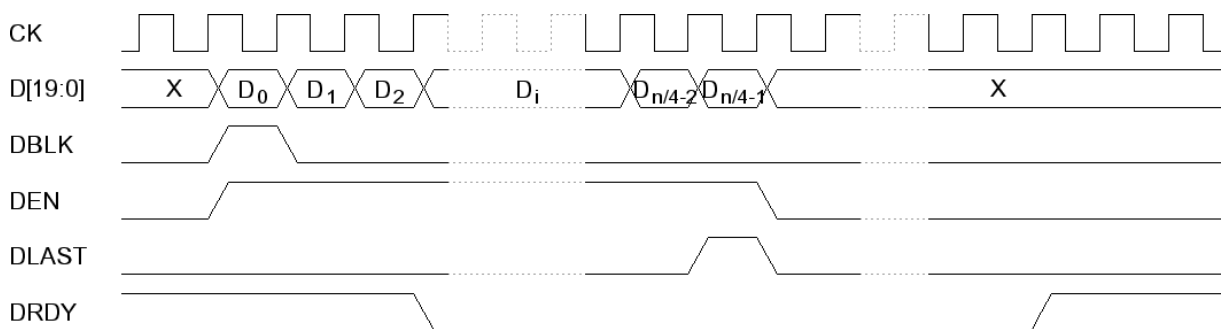


Figure 4: Input interface waveform example

Any additional "high" value on signal DBLK occurring between the valid pulse and the following DRDY rising is ignored.

3.3 Data output interface

3.3.1 Signals

Signal name	Type	Size	Function
Q	O	16	Decoded data. Format is described in section 3.3.2
QBLK	O	1	Block synchronization signal. Active HIGH. QBLK is asserted HIGH synchronously with the first valid decoded data.
QEN	O	1	Enable for Q Active HIGH
QLAST	O	1	End of block synchronization signal. Active HIGH. QLAST is asserted HIGH synchronously with the last decoded data.
QRDY	I	1	Ready for output signal. Active HIGH. HIGH indicates that a data can be output. LOW imposes to delay the output of a decoded data: QEN will mimic the QRDY waveform after a seven (7) clock cycles latency. Tie HIGH if not used.

Table 6: Output interface signals

3.3.2 Data size and format

Q is a 16 bit length signal. Q concatenates up to 16 user decoded bits.

Let denote by h_i the hard decision corresponding to the emitted systematic bit c_i . i is in $[0, k-1]$.

The output concatenated data $Q_j[15:0]$ is equal to

$$Q_j = h_{16j+15} \dots h_{16j+1} h_{16j}$$

The Table 7 gives the output data order for a block with rate $\frac{3}{4}$ and expansion factor 28. For this rate and code length, the last Q data contains partial Low Significant valid Bits.

symbol index	Q[15:0]
0	$h_{15} \dots h_1 h_0$
1	$h_{31} \dots h_{17} h_{16}$
..	
j	$h_{16j+15} \dots h_{16j+1} h_{16j}$
...	
31	$00000000 h_{16*31+7} h_{16*31+6} \dots h_{16*31}$

Table 7: Output data order (example: rate $\frac{3}{4}$, expansion factor 28)

According to the expansion factor and code rate, the last hard decoded word may contain only partial valid bits. The number of output word is

$$m = \left\lceil \frac{k}{16} \right\rceil, \text{ i.e. } m = \frac{k}{16} \text{ when } k \bmod 16 = 0 \text{ or } m = \frac{k}{16} + 1 \text{ when } k \bmod 16 \neq 0. \text{ In this last case,}$$

only $k \bmod 16$ bits are valid in the LSB part of the Q word.

3.3.3 Waveform examples

Figure 5 displays the general waveform for the output interface. The pattern of QRDY is arbitrary chosen. QEN reflects modification on QRDY after a latency of seven (7) clock cycles.

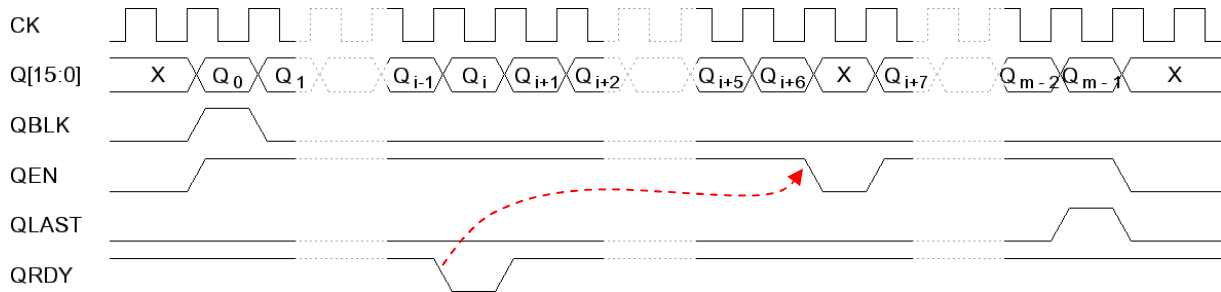


Figure 5: Output interface waveform example

3.4 Data Sequence

This section summarizes through an example what the input and output data sequences are. Section 3.2.2 (resp. section 3.3.2) describes the data format for input (resp. output) interface. Notations used in these sections also apply in this section.

Example

Let us consider the LDPC code for the rate $\frac{3}{4}$. A code with an expansion factor equal to 60. 1440 coded bits are emitted and 1440 soft LLR bits are provided as input. 1080 bits are user bits, 360 bits are redundancy bits.

The input word is

$$s_0 s_1 \dots s_{1078} s_{1079} s_{1080} \dots s_{1439}$$

Then, the input sequence shall be:

D: $D_0(s_0 s_1 s_2 s_3) D_1(s_4 s_5 s_6 s_7) \dots D_{359}(s_{1436} s_{1437} s_{1438} s_{1439})$

And the output sequence will be (only user bits):

Q: $Q_0(h_{15} \dots h_0) Q_1(h_{31} \dots h_{16}) \dots Q_{68}(\dots h_{1079} \dots h_{1072})$

symbol index	D[19:15]	D[14:10]	D[9:0]	D[4:0]
0	s_0	s_1	s_2	s_3
1	s_4	s_5	s_6	s_7
..				
i	s_{4i+3}	s_{4i+2}	s_{4i+1}	s_{4i}
...				
359	s_{1436}	s_{1437}	s_{1438}	s_{1439}

Table 8: input sequence for rate $\frac{3}{4}$, 1440 coded bits

symbol index	Q[15:0]
0	$h_{15}...h_1h_0$
1	$h_{31}...h_{17}h_{16}$
..	
j	$h_{16j+15}...h_{16j+1}h_{16j}$
...	
68	$00000000h_{1079}h_{1078}...h_{1072}$

Table 9: output sequence for rate $\frac{3}{4}$, 1440 coded bits

3.5 Configuration and monitoring interface

The configuration and monitoring interface is made of 7 dedicated signals.

3.5.1 Signals

Signal name	Type	Size	Function
ITSTOP	I	1	Stopping criterion enable flag HIGH: enables the stopping criterion LOW: disables the stopping criterion
ITMAX	I	8	Max iteration number. Unsigned value. Range from 1 to 255
RATE	I	3	Rate signal: "000" for rate = 1/2 "010" for rate = 2/3 A "011" for rate = 2/3 B "100" for rate = 3/4 A "101" for rate = 3/4 B "110" for rate = 5/6
EXP_FACT_INDEX	I	5	Index for expansion factor. Unsigned value Range from 0 to 18 Current expansion factor is $24 + 4 \cdot \text{EXP_FACT_INDEX}$

Table 10: Configuration interface signals

Table 11 provides the actual correspondence between the EXP_FACT_INDEX configuration signal and the expansion factor and the coded block size in bits.

Note: ITSTOP and ITMAX are internally disabled. Changing these values does not change internal processing.

EXP_FACT_INDEX	Expansion factor	Coded block size (bits)
0	24	576
1	28	672
2	32	768
3	36	864
4	40	960
5	44	1056
6	48	1152
7	52	1248
8	56	1344
9	60	1440
10	64	1536
11	68	1632
12	72	1728
13	76	1824
14	80	1920
15	84	2016
16	88	2112
17	92	2208
18	96	2304

Table 11: Expansion factor and index correspondence

Signal name	Type	Size	Function
SYNDOK	O	1	Flag for code word syndrome: - 1: output word is a valid code word - 0: output word is not a valid code word
IDLE	O	1	Flag: - 1: the core is idle - 0: the core is busy This flag might be useful for power management
ITDONE	O	8	DISABLE. Set to 0

Table 12: monitoring interface signals

3.5.2 Protocol

The configuration is registered synchronously with a valid DBLK flag. Figure 6 illustrates the configuration protocol. R_0 , It_0 , Ef_0 (resp. R_1 , It_1 , Ef_1) are linked to block #0 (resp. block #1)

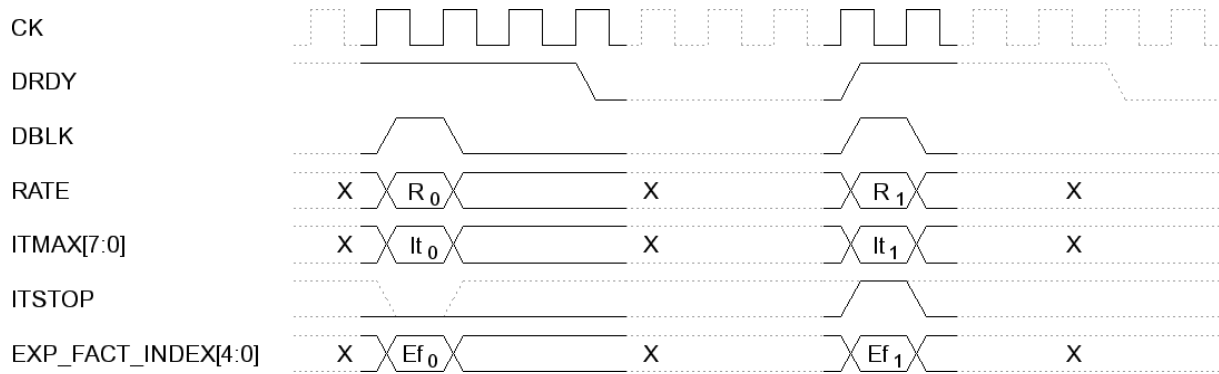


Figure 6: Configuration waveform

References

- [1] IEEE Std 802.16e-2005 and IEEE std 802.16-2004/Cor1-2005 “PART 16: Air Interface for Fixed and Mobile Broadband Wireless Access Systems – Amendment 2: Physical and Medium Access Control Layers for Combined Fixed and Mobile Operation in Licensed Bands – Corrigendum 1” IEEE Computer Society and IEEE Microwave Theory and Techniques Society, Feb.
- [2] TC4200_an1_Xilinx_implementations or TC4200_an2_Altera_implementations
- [3] TC4200_an4_ASIC_implementation_figures
- [4] TC4200_an0_BER_FER_performances