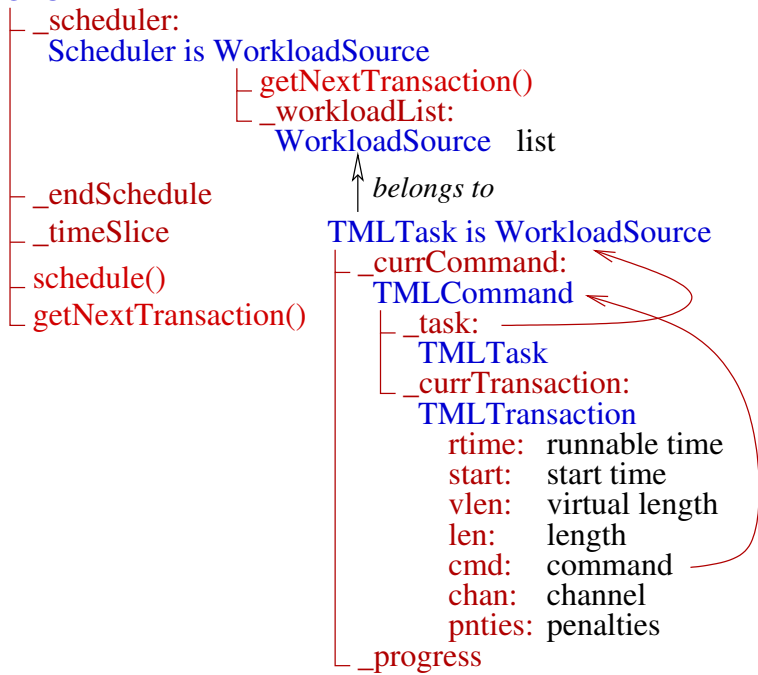


Synthetic and simplified view of the global class hierarchy

CPU



Data Channels

mapped on bus pathes, i.e. sequences of **BusMasters**

- one for reading
- one for writing

```
getFirstMaster(trans.)
```

```
getNextMaster(trans.)
```

BusMasters

accessGranted()

bus (list of)	<i>calls</i>
---------------	--------------

Bus

`_schedule()` *calls*

```
_calcStartTimeLength()
```

LcalcLength()

- *calcStartTimeLength* updates *transaction*'s start and *vlen*
- *calcLength* updates *transaction*'s *len*